PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

keeping a running history, up to a predetermined length, of power control instructions included in a first plurality frames received in one direction on a link of a channel, the first frames being queued before processing; and

generating power control commands for a second plurality of frames to be transmitted on a return direction of the channel, based at least in part on the running history being kept, in a manner that effectuates a slowing of response to the incoming power control instructions, the second frames also being batched for subsequent processing in batch form for transmission, wherein the power control instructions and commands are in a form of power control bits, and the predetermined length equals two bits and wherein the generating step comprises generating *m* "zero" value power control bits and *n* "one" value power control bits for each batch formed with a subset of the second frames, with *m* and *n* differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", *m* and *n* being integers.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The method of claim ~~3~~ 1, wherein if each batch of the subset of the second frames contains an even number of frames, *m* and *n* are equal.

5. (Currently Amended) The method of claim ~~3~~ 1, wherein if each batch of the subset of the second frames contains an odd number of frames, *m* and *n* differ by 1.

6. (Original)The method of claim 5, wherein m is greater than n by 1 for batches of odd ordinal positions in their order of formation, and n is greater than m by 1 for batches of even ordinal positions in their order of formation.

7. (Currently Amended) The method of claim 5, wherein m is greater than n by 1 for batches of even ordinal positions in their order of formation, and n is greater than m by 1 for batches of odd ordinal positions in their order of formation. .

8. (Currently Amended) The method of claim ~~2~~ 1, wherein said generating comprises alternating between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11".

9. (Original)The method of claim 8, wherein the last frame receives a "one" value power control bit, if there are odd number of frames in each batch, and the last two frames receive a "one" value power control bit, if there are even number of frames in each batch. .

10. (Currently Amended) The method of claim ~~2~~ 1, wherein said generating comprises alternating between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00".

11. (Original) The method of claim 10, wherein the last frame receives a "zero" value power control bit, if there are odd number of frames in each batch, and the last two frames receive a "zero" value power control bit, if there are even number of frames in each batch.

12. (Original) The method of claim 1, wherein said keeping and generating operations are being performed in a gateway of a wireless communication system.

13. (Original) The method of claim 1, wherein said keeping and generating operations are being performed in an emulated gateway and a gateway simulator of a wireless communication test system.

14. (Original) A gateway of a wireless communication system, comprising:

a transceiver to receive a first plurality frames on a first link of a channel, and batch said first frames for processing in batch, each of said first frames include a power control instruction, and the transceiver outputting the power control instruction included in each of said first frames;

a processing subsystem coupled to the transceiver subsystem to process the batched first frames in batch and to receive the power control instructions of the first frames outputted by the transceiver subsystem, and to generate a second plurality of frames for a second link of the channel, the second plurality of frames also being batched before being handled by the transceiver subsystem in batch, wherein the processing subsystem:

keeps a running history, up to a predetermined length, of the power control instructions included in the first frames, and

generate power control commands for the second frames based at least in part on the running history being kept, in a manner that effectuates slowing of responding to the incoming power control instructions.

15. (Original) The gateway of claim 14, wherein the power control instructions are in a form of power control bits, and the predetermined length equals two bits.

16. (Original) The gateway of claim 15, wherein the processing subsystem is designed to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second frames, with m and n differ by at most 1, if the two bits running history equals a selected one of "01" and "10", m and n being integers.

17. (Original) The gateway of claim 16, wherein the processing subsystem is designed to generate equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames.

18. (Original) The gateway of claim 16, wherein the processing subsystem is designed to generate a selected one of one more "zero" value power control bit and one more "one" value power control bit, if each batch of the subset of the second frames contains an odd number of frames.

19. (Original) The gateway of claim 18, wherein the processing subsystem is designed to generate one more "zero" value power control bit for batches of odd ordinal positions in their order of formation, and one more "one" value power control bit for batches of even ordinal positions in their order of formation.

20. (Currently Amended) The gateway of claim 18, wherein the processing subsystem is designed to generate one more "zero" value power control bit for batches of even ordinal positions in their order of formation, and one more "one" value power control bit for batches of odd ordinal positions in their order of formation.

21. (Original) The gateway of claim 15, wherein the processing subsystem is designed to alternate between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11".

22. (Currently Amended) The gateway of claim 21, wherein the processing subsystem is designed to generate the last frame with a "one" value power control bit, if there are odd number of frames in each batch, and the last two frames with a "one" value power control bit, if there are even number of frames in each batch.

23. (Original) The gateway of claim 15, wherein the processing subsystem is designed to alternate between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00".

24. (Currently Amended) The gateway of claim 23, wherein the processing subsystem is designed to generate the last frame with a "zero" value power control bit, if there are odd number of frames in each batch, and the last two frames with a "zero" value power control bit, if there are even number of frames in each batch.

25. (Currently Amended) A wireless communication testing system, comprising:

a gateway emulator to emulate a gateway including receipt of a first plurality frames in one direction on a link of a channel, and queueing said first frames for processing in batch, each of said first frames including a power control instruction, and the gateway emulator outputting the power control instruction included in each of said first frames;

a gateway simulator coupled to the gateway emulator to process the grouped first frames in batch and to receive the power control instructions of the first frames output by the gateway emulator, and to generate a second plurality of frames for transfer in an opposite direction on a link of the channel, the second plurality of frames also being batched before being handled by the gateway emulator in batch, wherein the gateway simulator:

maintains a running history over a predetermined length, of the power control instructions included with the first frames, and

generates power control commands for the second frames based at least in part on the running history being kept, in a manner that effectuates a slowing of response to the incoming power control instructions.

26. (Original) The wireless communication testing system of claim 25, wherein the power control instructions and commands are in a form of power control bits, and the predetermined length equals two bits.

27. (Original) The wireless communication testing system of claim 26, wherein the gateway simulator is designed to generate *m* "zero" value power control bits and *n* "one" value power control bits for each batch formed with a subset of the second frames, with *m* and *n* differ by at most 1, if the two bits running history equals a selected one of "01" and "10", *m* and *n* being integers.

28. (Original) The wireless communication testing system of claim 27, wherein the gateway simulator is designed to generate equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames.

29. (Original) The wireless communication testing system of claim 27, wherein the gateway simulator is designed to generate a selected one of one more "zero" value power control bit and one more "one" value power control bit, if each batch of the subset of the second frames contains an odd number of frames.

30. (Original) The wireless communication testing system of claim 29, wherein the gateway simulator is designed to generate one more "zero" value power control bit for batches of odd ordinal positions in their order of formation, and one more "one" value power control bit for batches of even ordinal positions in their order of formation.

31. (Currently Amended) The wireless communication testing system of claim 29, wherein the gateway simulator is designed to generate one more "zero" value power control bit for batches of even ordinal positions in their order of formation, and one more "one" value power control bit for batches of odd ordinal positions in their order of formation.

32. (Original) The wireless communication testing system of claim 26, wherein the gateway simulator is designed to alternate between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second frames,

with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11".

33. (Currently Amended) The wireless communication testing system of claim 32, wherein the gateway simulator is designed to generate the last frame with a "one" value power control bit, if there are odd number of frames in each batch, and the last two frames with a "one" value power control bit, if there are even number of frames in each batch.

34. (Original) The wireless communication testing system of claim 26, wherein the gateway simulator is designed to alternate between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00".

35. (Original) The wireless communication testing system of claim 34, wherein the gateway simulator is designed to generate the last frame with a "zero" value power control bit, if there are odd number of frames in each batch, and the last two frames with a "zero" value power control bit, if there are even number of frames in each batch.

36. (Currently Amended) Apparatus comprising:

means for keeping a running history, up to a predetermined length, of power control instructions included in a first plurality frames received on a first link of a channel, the first frames being grouped before their processing; and

means for generating power control commands for a second plurality of frames to be transmitted on a second link of the channel, based at least in part on the running history being kept, in a manner that effectuate slowing response to the incoming power control instructions, the second frames also being grouped for subsequent processing in batch for transmission, wherein the power control instructions and commands are in a form of power control bits, and the predetermined length equals two bits and wherein the means for generating power comprises generating m "zero" value power control bits and n "one" value power control bits for each batch

formed with a subset of the second frames, with *m* and *n* differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", *m* and *n* being integers.

37. (Currently Amended) A machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising:

keeping a running history, up to a predetermined length, of power control instructions included in a first plurality frames received on a first link of a channel, the first frames being grouped before their processing; and

generating power control commands for a second plurality of frames to be transmitted on a second link of the channel, based at least in part on the running history being kept, in a manner that effectuate slowing response to the incoming power control instructions, the second frames also being grouped for subsequent processing in batch for transmission, wherein the power control instructions and power control commands are in a form of power control bits, and the predetermined length equals two bits and wherein the generating step comprises generating *m* "zero" value power control bits and *n* "one" value power control bits for each batch formed with a subset of the second frames, with *m* and *n* differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", *m* and *n* being integers.

38. (Currently Amended) A machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising:

emulating a gateway including receipt of a first plurality frames on a first link of a channel, and grouping said first frames for processing in batch form, each of said first frames including a power control instruction, and outputting the power control instruction includes in each of said first frames;

a gateway simulator coupled to the gateway emulator to process the batched first frames in batch and to receive the power control instructions of the first frames outputted by the gateway emulator, and to generate a second plurality of frames for a second link of the channel, the second plurality of frames also being batched before being handled by the gateway emulator in batch, wherein the gateway simulator

keeps a running history, up to a predetermined length, of the power control instructions included in the first frames, and

generate power control commands for the second frames based at least in part on the running history being kept, in a manner that effectuates slowing of responding to the incoming power control instructions, wherein the power control instruction and power control commands are in a form of power control bits, and the predetermined length equals two bits and wherein the generating step comprises generating *m* "zero" value power control bits and *n* "one" value power control bits for each batch formed with a subset of the second frames, with *m* and *n* differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", *m* and *n* being integers.